Hardware/Software, Design/Verification, Security · Bordeaux, France · contact@jcert.es · +33 9 72 64 90 98

Jonathan Certes | Resume

R&D Engineer - Formal verification | 10 years experience

- Status: Ph.D - verification of critical embedded systems
- Activity: Design, Verification, Research, Teaching
- Programming: C/C++, Assembly, Python, Tcl/Tk
- Modelling: Verilog/VHDL, LTL/PSL, Coq, Spice, SystemC
- Hardware: FPGA, *System on Chip* Xilinx Zynq-7000, { AXI, SPI, I2C, UART }

Experience

R&D Engineer - Formal verification (*Keysom*, Bordeaux, France) 2024-Present

- Formal verification: RISC-V processor architectures
- Design / Modelling / Verification: SystemVerilog, Coq, Python

Teaching assistant (University of Toulouse / University of Bordeaux) 2019-Present

- { Software, Hardware, Network } security
- Operating systems, Hardware architectures

Ph.D. student: formal verification of systems (University of Toulouse) 2019-2023

- Formally verified remote attestation on microprocessors
- Automated formal verification of hardware designs

Hardware/Software engineer (*BiBench Systems*, Toulouse, France) 2017-2019

- Research and development: ageing of hardware devices for satellites (CNES contract)
- Design / Modelling / Verification: embedded C, VHDL, PCB

Hardware engineer (*Dolphin Integration*, Grenoble, France) 2012-2017

- Research and development: *crosstalk* / SNR performances for PWM converters
- Design / Modelling / Verification: Spice, VHDL, Verilog

Research activity **technical details** @ https://jcert.es/research/

Education

Ph.D. degree (University of Toulouse, France) 2019-2023

- Thesis: *Methods and models for formal verification of remote attestation on microprocessors*
- Model-checking and proof of security for hardware/software co-designs

Master of Science (M.S.) degree (University of Bordeaux, France) 2007-2011

- Research degree, specializing in electronics with high honors
- Bordeaux Graduate School of Engineering, specializing in electronics (ENSEIRB) with honors

CPGE: 2 years intensive Maths and Physics course (Brive, France) 2005-2007

- Preparation to selective entrance examination: enrolment to French engineering schools
- National competitive exams (ranked 34 on 850)

Time spent abroad (internships) 2010-2011

- *ColArt Ltd*, London, England (3 months)
- *LCCI-UFBA*: Integrated Circuits Design Laboratory, Salvador da Bahia, Brazil (8 months)