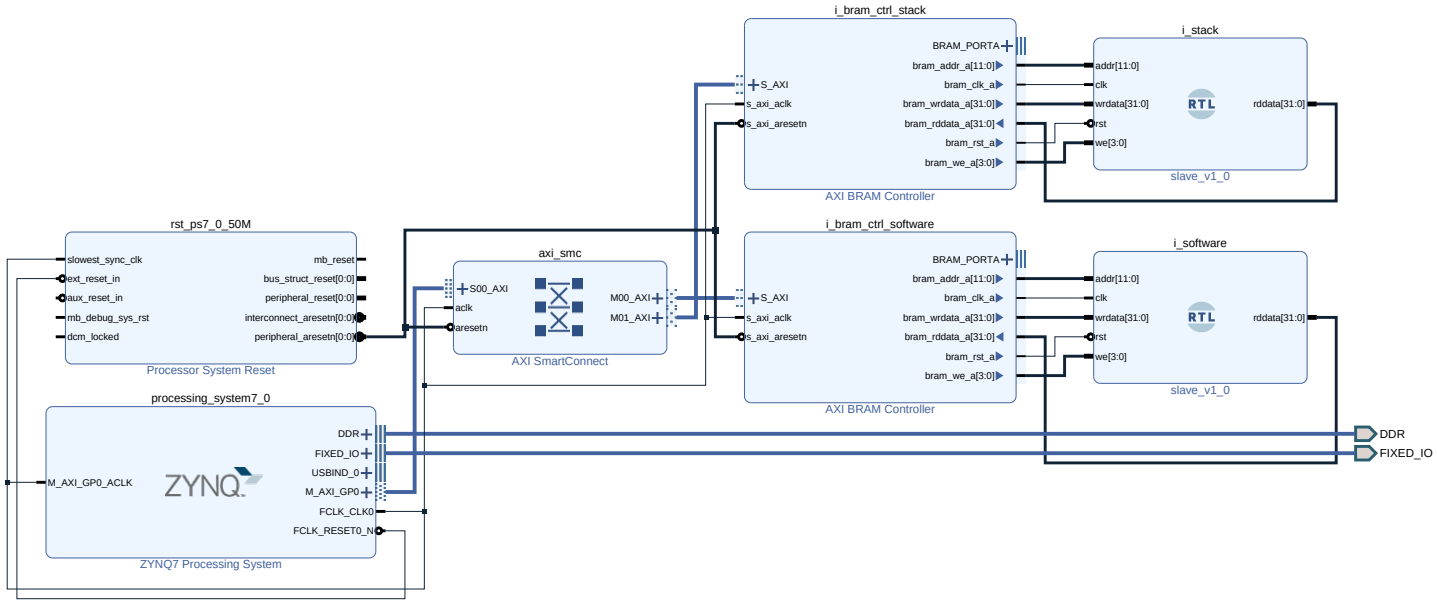
i_bram_ctrl_stack
BRAM_PORTA
bram_addr_a[11:0]
bram_clk_a
bram_wrdata_a[31:0]
bram_rddata_a[31:0]
bram_rst_a
bram_we_a[3:0]
S_AXI
s_axi_aclk
s_axi_aresetn
AXI BRAM Controller
i_stack
addr[11:0]
clk
wrdata[31:0]
rst
we[3:0]
rddata[31:0]
RTL
slave_v1_0
rst_ps7_0_50M
slowest_sync_clk
ext_reset_in
aux_reset_in
mb_debug_sys_rst
dcm_locked
mb_reset
bus_struct_reset[0:0]
peripheral_reset[0:0]
interconnect_aresetn[0:0]
peripheral_aresetn[0:0]
Processor System Reset
axi_smc
S00_AXI
aclk
aresetn
M00_AXI
M01_AXI
AXI SmartConnect
i_bram_ctrl_software
BRAM_PORTA
bram_addr_a[11:0]
bram_clk_a
bram_wrdata_a[31:0]
bram_rddata_a[31:0]
bram_rst_a
bram_we_a[3:0]
S_AXI
s_axi_aclk
s_axi_aresetn
AXI BRAM Controller
i_software
addr[11:0]
clk
wrdata[31:0]
rst
we[3:0]
rddata[31:0]
RTL
slave_v1_0
processing_system7_0
M_AXI_GP0_ACLK
ZYNQ
DDR
FIXED_IO
USBIND_0
M_AXI_GP0
FCLK_CLK0
FCLK_RESET0_N
ZYNQ7 Processing System
DDR
FIXED_IO